

- 1           1.    A method comprising:  
2                   chemical mechanical polishing through a portion  
3 of an insulating third layer down to a conductive second  
4 layer coated on a first layer having an opening filled at  
5 least in part by said third layer.
- 1           2.    The method of claim 1 including chemical  
2 mechanical polishing through the second layer down to the  
3 first layer.
- 1           3.    The method of claim 1 including forming an  
2 insulating first layer.
- 1           4.    The method of claim 3 including covering said  
2 first layer with a second layer having a high planarization  
3 selectivity relative to the third layer.
- 1           5.    The method of claim 1 including forming the first  
2 layer of oxide and the second layer of tungsten.
- 1           6.    The method of claim 5 including forming the third  
2 layer of high density plasma oxide.
- 1           7.    The method of claim 1 including conformally  
2 coating the walls of said opening with said second layer.

1           8.    The method of claim 1 including forming the third  
2 layer of material having lower thermal conductivity than  
3 thermally grown oxide.

1           9.    The method of claim 1 including polishing down to  
2 said second layer, stopping, and then polishing through a  
3 portion of said second layer.

1           10.   A semiconductor structure comprising:  
2                a dielectric material formed over a substrate,  
3 said dielectric material having an aperture formed at least  
4 partially through said dielectric material;  
5                a conductive material conformally coated over  
6 said dielectric and said aperture; and  
7                a thermally insulating material formed within  
8 said aperture over said conductive material.

1           11.   The structure of claim 10 wherein said conductive  
2 material is tungsten and said insulating material is a high  
3 density plasma oxide.

1           12.   The structure of claim 10 wherein said conductive  
2 material has high polishing selectivity relative to said  
3 insulating material.

1        13. The structure of claim 10 wherein said insulating  
2 material has a lower thermal conductivity than thermally  
3 grown oxide.

1        14. A method comprising:  
2                chemical mechanical polishing through a portion  
3 of a thermally insulating third layer down to a conductive  
4 layer coated on a first layer having an opening filled at  
5 least in part with said third layer;  
6                forming a pair of spaced electrodes so that one  
7 of said electrodes is coupled to said conductive layer; and  
8                forming a memory material between said  
9 electrodes.

1        15. The method of claim 14 including forming an  
2 electrical contact electrically coupled to a conductive  
3 line formed in said substrate.

1        16. The method of claim 14 including forming the  
2 conductive layer by conformally coating said first layer  
3 with a conductive material.

1        17. The method of claim 16 including coating said  
2 first layer with tungsten.

1        18. The method of claim 14 including forming a  
2 thermally insulating filler in said opening.

1        19. The method of claim 14 including planarizing  
2 through said thermally insulating third layer using said  
3 conductive layer as a planarization stop.

1        20. The method of claim 19 including stopping the  
2 planarizing at said conductive layer and then polishing  
3 through said conductive layer to said first layer.

1        21. The method of claim 14 including planarizing so  
2 as to have high selectivity to the conductive layer  
3 relative to said third layer.

1        22. The method of claim 14 including forming a phase  
2 change memory material between said electrodes.

1        23. The method of claim 22 including forming a  
2 chalcogenide between said electrodes.

1        24. A memory comprising:  
2            an electrical contact coupled to a line in a  
3 substrate;

4           a tubular conductor extending upwardly from said  
5     contact, said tubular conductor being filled with a  
6     thermally insulating material;  
7           a lower electrode coupled to said tubular  
8     electrode;  
9           a memory material over said lower electrode; and  
10          an upper electrode over said memory material.

1           25. The memory of claim 24 wherein said memory  
2     material is a phase change material.

1           26. The memory of claim 25 wherein said phase change  
2     material is a chalcogenide.

1           27. The memory of claim 24 wherein said tubular  
2     conductor is formed at least in part of tungsten.

1           28. The memory of claim 24 wherein said thermally  
2     insulating material has a thermal conductivity lower than  
3     that of thermally grown oxide.

1           29. A system comprising:  
2           a processor-based device;  
3           a wireless interface coupled to said processor-  
4     based device; and

5           a semiconductor memory coupled to said device,  
6   said memory including a substrate, said substrate including  
7   a conductive line, a contact formed over said substrate  
8   electrically coupled to said conductive line, and a memory  
9   element over said contact, said memory element coupled to  
10   said contact by a tubular conductor filled with a thermally  
11   insulating material.

1           30. The system of claim 29 wherein said memory  
2   material is a phase change material.

1           31. The system of claim 30 wherein said phase change  
2   material is a chalcogenide.

1           32. The system of claim 29 wherein said tubular  
2   conductor is formed at least in part of tungsten.

1           33. The system of claim 29 wherein said thermally  
2   insulating material has a thermal conductivity lower than  
3   that of thermally grown oxide.